27 papers

Modeling process variation and wear-out (2 lectures):
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1a) "VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects", by Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, IEEE Transactions on Semiconductor Manufacturing (IEEE TSM), February 2008.

1b) "Facelift: Hiding and Slowing Down Aging in Multicores", by Abhishek Tiwari and Josep Torrellas, International Symposium on Microarchitecture (MICRO), November 2008.

Tolerating/mitigating variation with body biasing (1 lecture)
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2a) "Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing" by Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, International Symposium on Microarchitecture (MICRO), December 2007.

Tolerating/mitigating variation with timing speculation (2 lectures)
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3a) "Razor: A lowpower pipeline based on circuit-level timing speculation. In International Symposium on Microarchitecture", by D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, C. Zeisler, D. Blaauw, T. Austin, K. Flautner, and T. Mudge, International Symposium on Microarchitecture (MICRO), 2003.

3b) "BlueShift: Designing Processors for Timing Speculation from the Ground Up" by Brian Greskamp, Lu Wan, Ulya R. Karpuzcu, Jeffrey J. Cook, Josep Torrellas, Deming Chen, and Craig Zilles, International Symposium on High-Performance Computer Architecture (HPCA), February 2009.

Tolerating/mitigating variation with application scheduling (1 lecture)
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4a) "Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors", by Radu Teodorescu and Josep Torrellas, International Symposium on Computer Architecture (ISCA), June 2008.

Reducing voltage guardbands (3 lectures)
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5a) "Near-Threshold Computing: Reclaiming Moore's Law Through Energy

Efficient Integrated Circuits", by Ronald G. Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvester, and Trevor Mudge. Proceedings of the IEEE, February 2010.

5b) "Active management of timing guardband to save energy in POWER7" by C. R. Lefurgy, A. J. Drake, M. S. Floyd, M. S. Allen-Ware, B. Brock, J. A. Tierno, and J. B. Carter. International Symposium on Microarchitecture (MICRO), December 2011.

5c) "Dynamic Reduction of Voltage Margins by Leveraging On-chip ECC in Itanium II Processors" by Anys Bacha and Radu Teodorescu, , International Symposium on Computer Architecture (ISCA), June 2013.

Managing voltage droops (1 lecture)
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6a) "Voltage Smoothing: Characterizing and Mitigating Voltage Noise in a Production Processor Using Software-Guided Thread Scheduling", by Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei, David Brooks, International Symposium on Microarchitecture (MICRO), Dec. 2010.

Design for low voltage (2 lectures)
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7a) "ScalCore: Designing a Core for Voltage Scalability" by Bhargava Gopireddy, Choungki Song, Josep Torrellas, Nam Sung Kim, Aditya Agrawal, and Asit Mishra, International Symposium on High Performance Computer Architecture (HPCA), March 2016.

7b) "Tangle: Route-Oriented Dynamic Voltage Minimization for Variation-Afflicted, Energy-Efficient On-Chip Networks", by Amin Ansari, Asit Mishra, Jianping Xu, and Josep Torrellas, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

Leakage (1 lecture)
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8a) "Drowsy Caches: Simple Techniques for Reducing Leakage Power", by Krisztian Flautner, Nam Sung Kim, Steve Martin, David Blaauw, Trevor Mudge, International Symposium on Computer Architecture (ISCA), June 2002.

Efficient DRAM/eDRAM design (3 lectures)
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9a) "Reducing cache power with low-cost, multi-bit error-correcting codes" by C. Wilkerson, A. R. Alameldeen, Z. Chishti, W. Wu, D. Somasekhar, and S.-L. Lu, International Symposium on Computer

Architecture (ISCA), 2010.

9b) "Mosaic: Exploiting the Spatial Locality of Process Variation to Reduce Refresh Energy in On-Chip eDRAM Modules", by Aditya Agrawal, Amin Ansari, and Josep Torrellas, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

9c) "An Experimental Study of Data Retention Behavior in Modern DRAM Devices: Implications for Retention Time Profiling Mechanisms" by J. Liu, B. Jaiyen, Y. Kim, C. Wilkerson, and O. Mutlu, , International Symposium on Computer Architecture (ISCA), 2013.

Power gating and microcheckpointing (1 lecture)
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10a) "NVSleep: Using Non-Volatile Memory to Enable Fast Sleep/Wakeup of Idle Cores" by Xiang Pan and Radu Teodorescu, International Conference on Computer Design (ICCD), October 2014.

Controllers (3 lectures)
==========

11a) "Using Multiple Input, Multiple Output Formal Control to Maximize Resource Efficiency in Architectures", by Raghavendra Pothukuchi, Amin Ansari, Petros Voulgaris, and Josep Torrellas, International Symposium on Computer Architecture (ISCA), June 2016.

11b) "Crank It Up or Dial It Down: Coordinated Multiprocessor Frequency and Folding Control" by Augusto Vega, Alper Buyuktosunoglu, Heather Hanson, Pradip Bose, Srinivasan Ramani, International Symposium on Microarchitecture (MICRO), 2013.

11c) "Scalably Verifiable Dynamic Power Management" by Opeoluwa Matthews, Meng Zhang, and Daniel J. Sorin, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

Temperature (1 lecture)
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12a) "Dynamic Thermal Management for High-Performance Microprocessors", by David Brooks, Margaret Martonosi,International Symposium on High-Performance Computer Architecture (HPCA), 2001.

3D stacked architectures (4 lectures)
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13a) "Die Stacking (3D) Microarchitecture" by B. Black, M. Annavaram, N. Brekelbaum, J. DeVale, L. Jiang, G. Loh, D. McCauley, P. Morrow, D. Nelson, D. Pantuso, P. Reed, J. Rupley,
S. Shankar, J. Shen, and C. Webb, International Symposium on

Microarchitecture (MICRO), Dec.2006.

13b) "Centip3De: A Cluster-Based NTC Architecture With 64 ARM Cortex-M3 Cores in 3D Stacked 130 nm CMOS", by David Fick, Ronald G. Dreslinski, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wieckowski, Gregory Chen, Trevor Mudge, David Blaauw, and Dennis Sylvester,
IEEE Journal of Solid-State Circuits, January 2013.

13c) "Enabling Interposer-based Disintegration of Multi-core Processors" by Ajaykumar Kannan, Natalie Enright Jerger, Gabriel H. Loh, International Symposium on Microarchitecture (MICRO), June 2015.

13d) "Designing Vertical Processors in Monolithic 3D", by Bhargava Gopireddy and Josep Torrellas, International Symposium on Computer Architecture (ISCA), June 2019.

Extreme scale architectures (1 lecture)
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14b) "Runnemede: An Architecture for Ubiquitous High-Performance Computing" by Nicholas P. Carter, Aditya Agrawal, Shekhar Borkar, Romain Cledat, Howard David, Dave Dunning, Joshua Fryman, Ivan Ganev, Roger A. Golliver, Rob Knauerhase, Richard Lethin, Benoit Meister, Asit K. Mishra, Wilfred R. Pinfold, Justin Teller, Josep Torrellas, Nicolas Vasilache, Ganesh Venkatesh, and Jianping Xu, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

Mobile systems (1 lecture)
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15a) "Mobile CPUs rise to power: Quantifying the impact of generational mobile CPU design trends on performance, energy, and user satisfaction" by M. Halpern, Y. Zhu, and V. J. Reddi, International Symposium on High Performance Computer Architecture (HPCA), March 2016.